GEORGIA INSTITUTE OF TECHNOLOGY

SCHOOL OF ELECTRICAL & COMPUTER ENGINEERING

ECE 2031: Digital Design Laboratory

Syllabus

Instructor:
Ashutosh Srivastava
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Office hours
Room 112b, 1st Floor, GTE Building
TBA

Class Details:
TBA

Prerequisites:
ECE 2020
ECE 2035 or 2036 (may be taken concurrently)

Course Materials:
Required Text:

Thomas R. Collins and Christopher M. Twigg
Digital Design Laboratory Manual (2nd Edition)
ISBN: 978-0757571572
An eBook option is available directly from the publisher.
You must purchase a new copy. (There are consumable pages.)

Optional Texts:

H. O. Hamblen, T. S. Hall, and M. D. Furman
Rapid Prototyping of Digital Systems: SOPC Edition
ISBN: 978-0387726700
Leslie C. Perelman, James Paradis, and Edward Barrett
The Mayfield Handbook of Technical & Scientific Writing
ISBN: 978-1559346474
(Available on-line at http://www.mhhe.com/mayfieldpub/tsw/home.htm)
ECE 2031 Workbook (available at the main course website)

Course Goals and Learning Outcomes:

The goal in ECE 2031 is to experience the conception, design, fabrication, and testing of digital hardware in a hands-on setting.

Laboratory projects will use a PC-based CAD tool environment that supports schematic capture, logic simulation, and VHDL-based logic synthesis on FPGAs (Field Programmable Gate Arrays). Discrete logic devices will be used for two designs, but VHDL-based logic synthesis on FPGA-based design boards will be used for more advanced design implementations. The semester will culminate with a design project specified and undertaken by teams of three students.

Course Objectives:

As described at https://www.ece.gatech.edu/courses/course_outline/ECE2031, the objectives for students are to:

1. Apply their knowledge from ECE 2020 (or CS 2110) to practical laboratory experience in digital computing systems.
2. Apply the concepts of basic combinational logic circuits, sequential circuit elements, and programmable logic in the laboratory setting.
3. Develop familiarity and confidence with designing, building and testing digital circuits, including the use of CAD tools.
4. Develop team-building skills and enhance technical knowledge through both written assignments and design projects.

Course Outcomes:

Also, from the ECE web site, upon successful completion of this course, students should be able to do the following:

- Implement combinational logic circuits both with TTL devices on a protoboard and within a complex PLD.
- Analyze the timing of digital circuits with oscilloscopes and logic analyzers.
- Design and implement state machines to meet design specifications.
- Design circuits with a graphical schematic CAD editor.
- Simulate circuits within a CAD tool and compare to design specifications.
- Design, implement, and simulate circuits using VHDL.
- Implement a simple computer within a PLD.
- Write machine language programs and assembly language programs for the simple computer.
- Use a complex sequential logic circuit as part of a solution to an open-ended design problem.

- Write laboratory reports and documentation conforming to technical writing standards.
- Work effectively as team members to develop and write a group report.
- Work effectively as team members to design an approved project.

Attendance Policy:

Attendance is expected for the lecture remote and live sessions and mandatory for all laboratory sessions. Any absence from an exam or laboratory session will result in a grade of zero, which may be made up at the discretion of the instructor.

In case of a health issue that prevents you taking an exam or returning an assessment, a note from a doctor will be required before rescheduling the exam otherwise you will have an F to the exam.

Grade Policy:

- 25 % Lab reports
- 25% Prelab quizzes
- 10 % One or more Lab Practical Exercises
- 20 % Final Project
- 20 % In-class Exam

All letter grade assignments are made by the instructor and are based on the ranking in each individual laboratory session. All assignments are individual assignments. This includes pre-lab work, laboratory reports, homework assignments, computer simulations, and exams. You will work in groups on the labs, but everything you turn in must be your own work.

The written exams are closed book and closed note. The lab practical exam is open book, open notes. The lab practical exam will be determined later in the semester. At the beginning of all exams, any electronic communication device must be turned off and put away for the duration of the exam.

Open Lab:

Hopefully you will complete all lab assignments during your allotted time. I have yet to decide whether or not it will be necessary to hold additional open lab hours.

Final Exam:

There is no final exam for this course. You will give a final project presentation during the lab session of dead week. The written final report will be due during finals week.

Academic Misconduct:

All students taking this course are required to strictly adhere to the Georgia Tech Honor Code, whose complete text may be found at http://honor.gatech.edu/content/2/the-honor-code. Any violations of the Code are considered academic misconduct and will be submitted to the Office of the Dean of Students for appropriate action.

Collaboration:

Students may discuss assignments in general terms with one another, but all work should be generated individually. Likewise, students may receive assistance on assignments from the course instructors. However, all of the assignments in this course are to be completed individually. Although there are laboratory partners, each assignment laboratory reports, homework problems, exams must reflect only the efforts of the student whose name appears on the assignment. Copying or allowing peers to copy all or portions of any assignment is considered plagiarism and is expressly forbidden.

Tentative schedule (subject to adjustements)

Week	Lecture	Lab
#1	Introduction	No lab
#2	Computer Aided Logic Design	Lab 1
#3	Discrete Circuits	Lab 2
#4	Circuit Characteristics	Lab 3
#5	State Machines (SMs) and VHDL I	Lab 4
#6	Review session / written exam	No Lab
#7	VHDL II and Sequential Timing	Lab 5
#8	Train Lab	Lab 6
#9	Simple Computer I	Lab 7
#10	Simple Computer II	Lab 8
#11	Practical Exam Review	Practical exam
#12	Final Project Introduction	Project work
#13	Proposals	Project work
#14	Written Exam Review	Design summary/project work
#15	In class Exam	Project work
#16	Presentation & Report Tips	Project demos/project work